

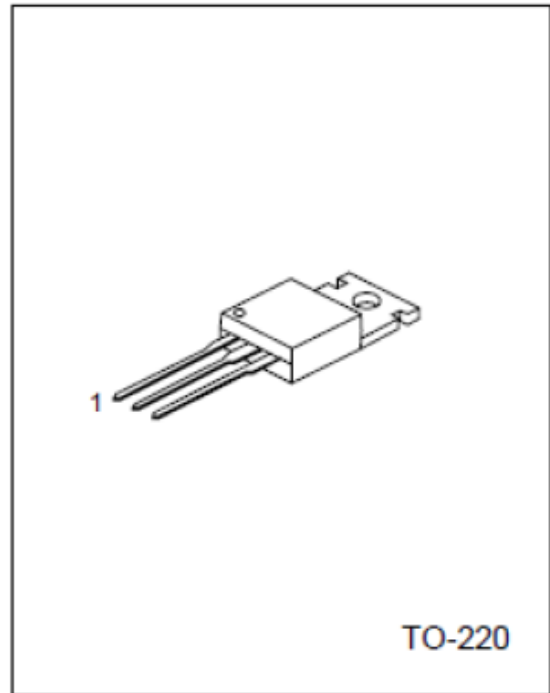
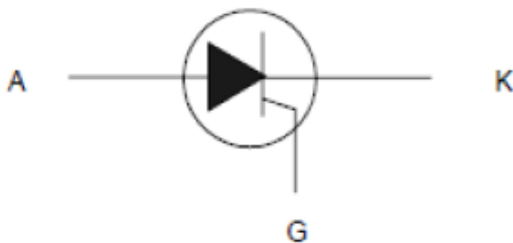


## SCRs

### DESCRIPTION

Passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

### SYMBOL



TO-220

1: CATHODE 2: ANODE 3: GATE

### ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	RATING	UNIT
Repetitive peak off-state voltages BT151-500 BT151-650 BT151-800	$V_{DRM}, V_{RRM}$	500* 650* 800	V
Average on-state current (half sine wave; $T_{mb} \leq 109^\circ\text{C}$ )	$I_{T(AV)}$	7.5	A
RMS on-state current (all conduction angles)	$I_{T(RMS)}$	12	A
Non-repetitive peak on-state current (half sine wave; $T_J = 25^\circ\text{C}$ prior to surge) $t = 10\text{ ms}$ $t = 8.3\text{ ms}$	$I_{TSM}$	100 110	A
$I^2t$ for fusing ( $t = 10\text{ ms}$ )	$I^2t$	50	$\text{A}^2\text{s}$
Repetitive rate of rise of on-state current after triggering ( $I_{TM} = 20\text{ A}$ ; $I_G = 50\text{ mA}$ ; $dI_G/dt = 50\text{ mA/ms}$ )	$dI_T/dt$	50	$\text{A}/\mu\text{s}$
Peak gate current	$I_{GM}$	2	A
Peak gate voltage	$V_{GM}$	5	V
Peak reverse gate voltage	$V_{RGM}$	5	V
Peak gate power (over any 20 ms period)	$P_{GM}$	5	W
Average gate power	$P_{G(AV)}$	0.5	W
Storage temperature	$T_{stg}$	-40~150	$^\circ\text{C}$
Operating junction temperature	$T_J$	125	$^\circ\text{C}$

\*Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed  $15\text{A}/\mu\text{s}$ .

## THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance Junction to mounting base	$R_{th\ j-mb}$			1.3	K/W
Thermal resistance Junction to ambient In free air	$R_{th\ j-a}$		60		K/W

STATIC CHARACTERISTICS( $T_J=25^\circ\text{C}$ , unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Gate trigger current	$I_{GT}$	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$		2	15	mA
Latching current	$I_L$	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$		10	40	mA
Holding current	$I_H$	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$		7	20	mA
On-state voltage	$V_T$	$I_T = 23\text{ A}$		1.4	1.75	V
Gate trigger voltage	$V_{GT}$	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$ $V_D = V_{DRM(max)}; I_T = 0.1\text{ A}; T_J = 125^\circ\text{C}$	0.25	0.6 0.4	1.5	V
Off-state leakage current	$I_D, I_R$	$V_D = V_{DRM(max)}; V_R = V_{RRM(max)};$ $T_J = 125^\circ\text{C}$		0.1	0.5	mA

DYNAMIC CHARACTERISTICS( $T_J=25^\circ\text{C}$ , unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Critical rate of rise of off-state voltage	$dV_D/dt$	$V_{DM} = 67\% V_{DRM(max)}; T_J = 125^\circ\text{C};$ exponential waveform; Gate open circuit $R_{GK} = 100\ \Omega$	50 200	130 1000		V/ $\mu\text{s}$
Gate controlled turn-on time	$t_{gt}$	$I_{TM} = 40\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$		2		$\mu\text{s}$
Circuit commutated Turn-off time	$t_{q}$	$V_D = 67\% V_{DRM(max)}; T_J = 125^\circ\text{C};$ $I_{TM} = 20\text{ A}; V_R = 25\text{ V}; dI_{TM}/dt = 30\text{ A}/\mu\text{s};$ $dV_D/dt = 50\text{ V}/\mu\text{s}; R_{GK} = 100\ \Omega$		70		$\mu\text{s}$

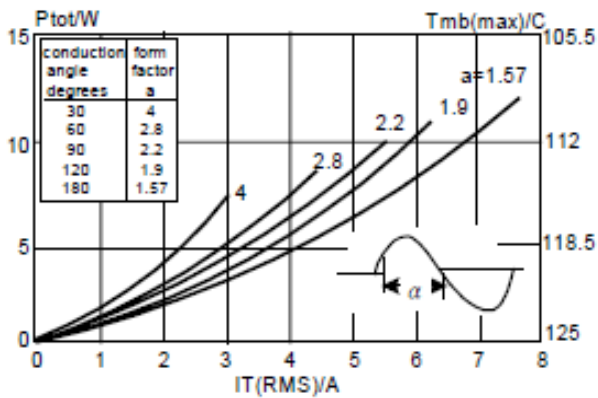


Fig. 1. Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$ .

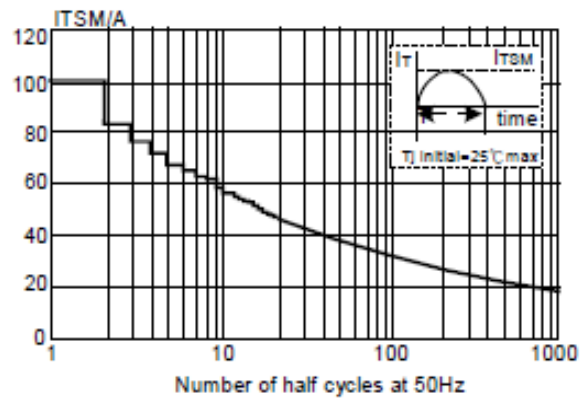


Fig. 4. Maximum Permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50\text{Hz}$ .

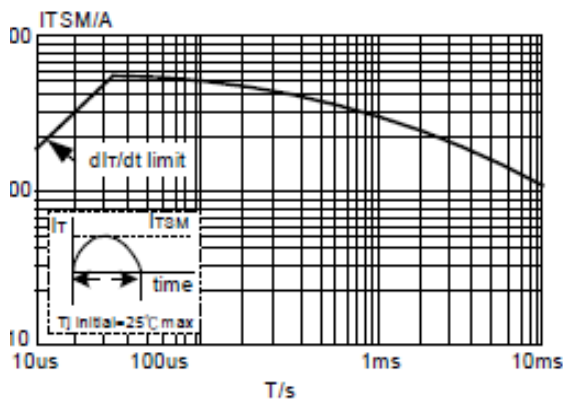


Fig. 2. Maximum Permissible non-repetitive peak on-state Current  $I_{TSM}$ , versus pulse width  $t_p$  for sinusoidal currents,  $t_p \leq 10\text{ms}$

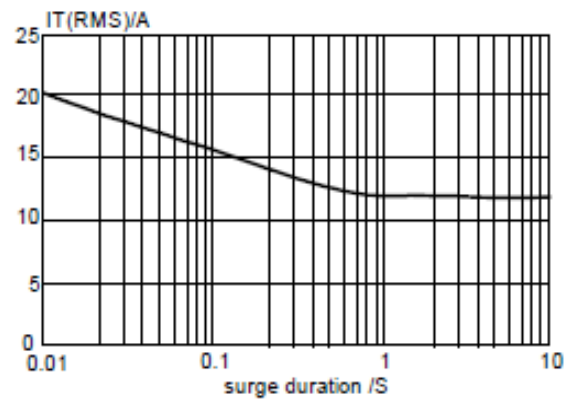


Fig. 5. Maximum permissible repetitive rms on-state current  $I_T(RMS)$ , versus surge duration, for sinusoidal currents,  $f = 50\text{Hz}$ ;  $T_{mb} \leq 109^\circ\text{C}$

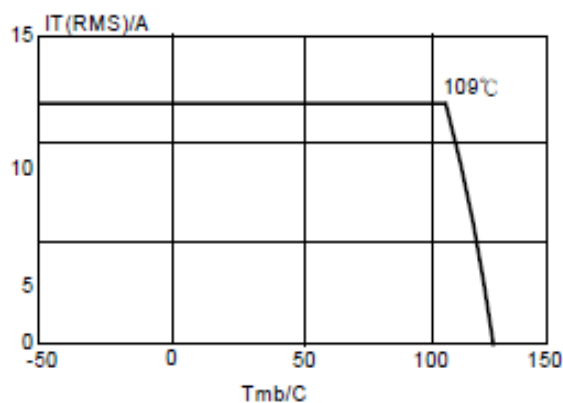


Fig. 3. Maximum permissible rms current  $I_T(RMS)$ , versus mounting base temperature  $T_{mb}$

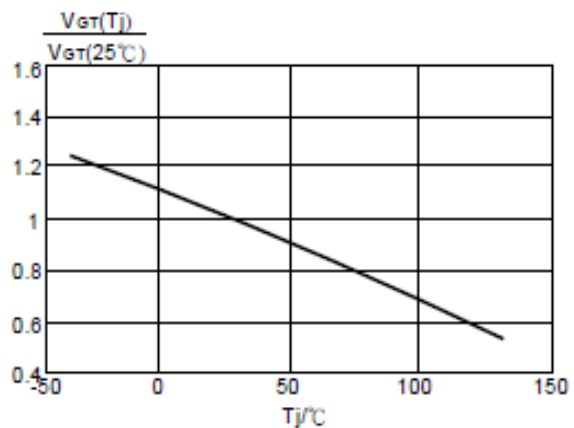


Fig. 6. Normalised gate trigger voltage  $V_{GT}(T) / V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

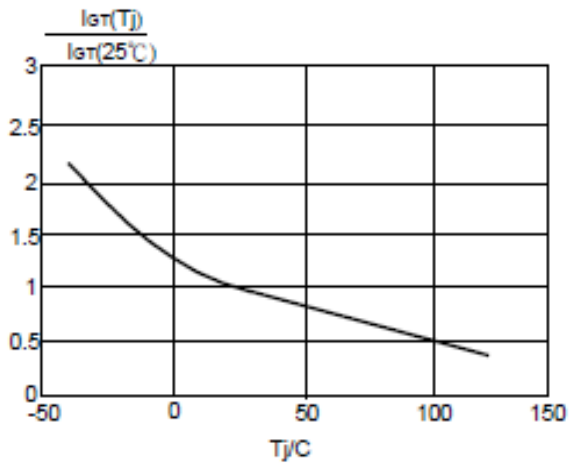


Fig. 7. Normalised gate trigger Current  $I_{gt}(T_j)/I_{gt}(25^\circ\text{C})$ , versus junction temperature  $T_j$

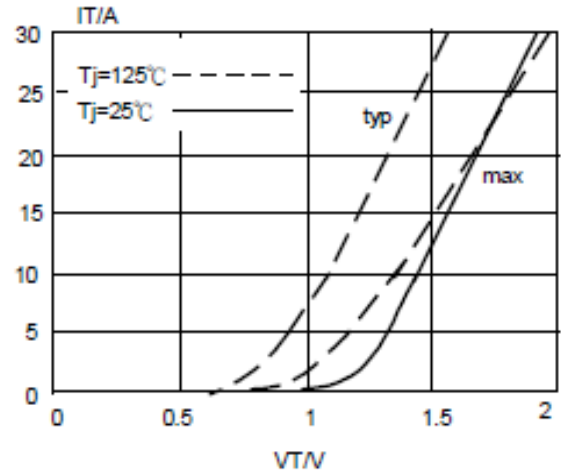


Fig. 10. Typical and maximum on-state characteristic.

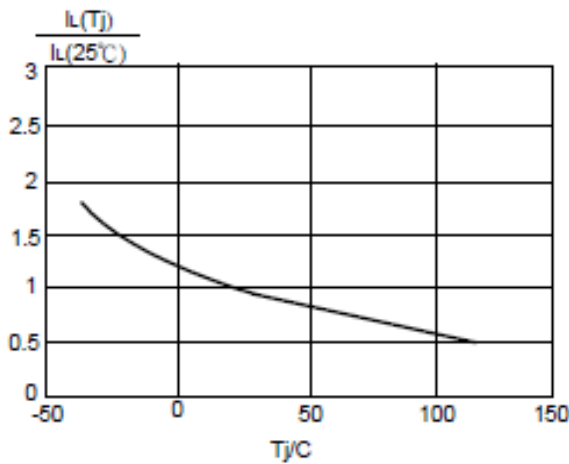


Fig. 8. Normalised latching Current  $I_l(T_j)/I_l(25^\circ\text{C})$ , versus junction temperature  $T_j$

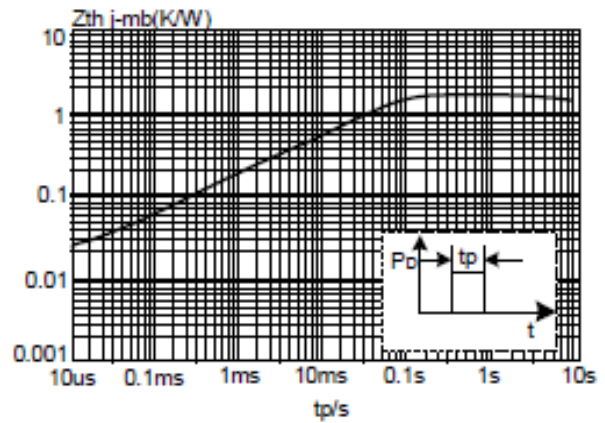


Fig. 11. Transient thermal impedance  $Z_{thj-mb}$ , versus pulse width  $t_p$ .

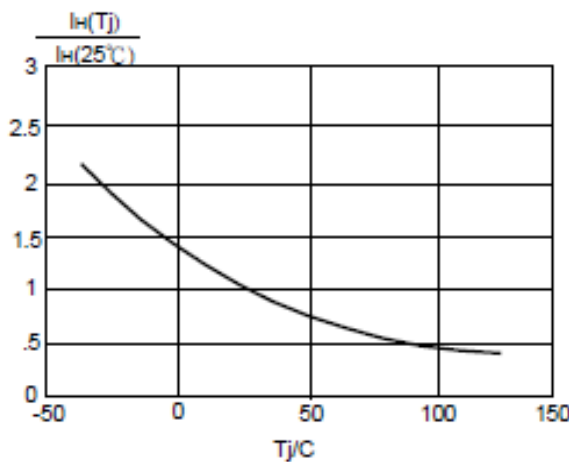


Fig. 9. Normalised holding current  $I_h(T_j)/I_h(25^\circ\text{C})$ , versus junction temperature  $T_j$

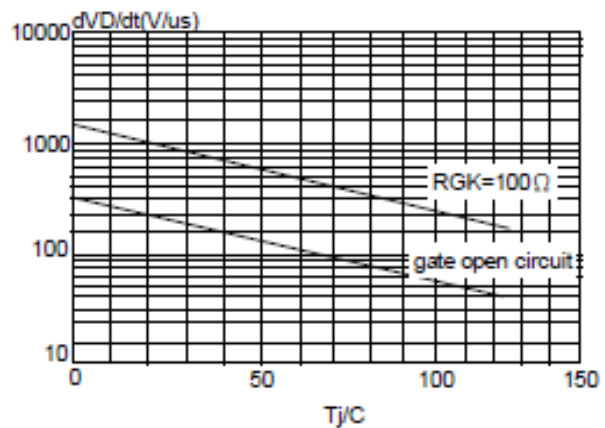


Fig. 12. Typical, critical rate of rise of off-state voltage,  $dV_o/dt$  versus junction temperature  $T_j$