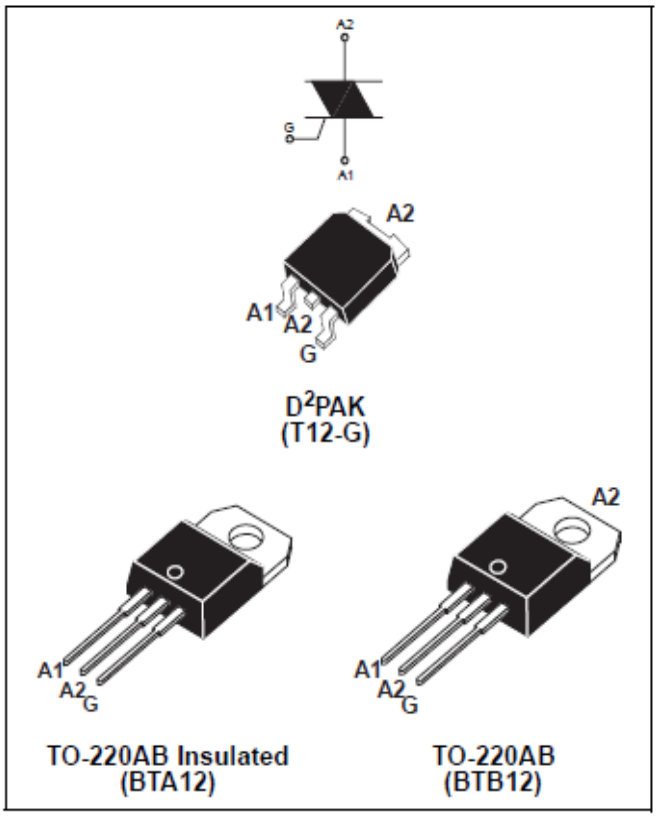
Wuxi Yaren Technology Co.,Ltd.

BTA/BTB12 Series

MAIN FEATURES:

Symbol	Value	Unit
$I_{T(RMS)}$	12	A
V_{DRM}/V_{RRM}	600 and 800	V
$I_{GT\ (Q_1)}$	5 to 50	mA



D²PAK (T12-G)

TO-220AB Insulated (BTA12)

TO-220AB (BTB12)

DESCRIPTION

Available either in through-hole or surface-mount packages, the BTA/BTB12 and T12 triac series is suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control operation in light dimmers, motor speed controllers,...

The snubberless versions (BTA/BTB...W and T12 series) are specially recommended for use on inductive loads, thanks to their high commutation performances. Logic level versions are designed to interface directly with low power drivers such as microcontrollers. By using an internal ceramic pad, the BTA series provides voltage insulated tab (rated at 2500V RMS) complying with UL standards (File ref.: E81734)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	D²PAK/TO-220AB	Tc = 105°C	12	A
		TO-220AB Ins.	Tc = 90°C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, Tj initial = 25°C)	F = 50 Hz	t = 20 ms	120	A
		F = 60 Hz	t = 16.7 ms	126	
I^2t	I^2t Value for fusing	tp = 10 ms		78	A^2s
dI/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, tr ≤ 100 ns	F = 120 Hz	Tj = 125°C	50	A/µs
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage	tp = 10 ms	Tj = 25°C	V_{DRM}/V_{RRM} + 100	V
I_{GM}	Peak gate current	tp = 20 µs	Tj = 125°C	4	A
$P_{G(AV)}$	Average gate power dissipation		Tj = 125°C	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	°C

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise specified)

■ SNUBBERLESS™ and LOGIC LEVEL (3 Quadrants)

Symbol	Test Conditions	Quadrant		T12		BTA/BTB12			Unit
				T1235	TW	SW	CW	BW	
I_{GT} (1)	V_D = 12 V R_L = 30 Ω	I - II - III	MAX.	35	5	10	35	50	mA
V_{GT}		I - II - III	MAX.	1.3					V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ Tj = 125°C	I - II - III	MIN.	0.2					V
I_H (2)	I_T = 100 mA		MAX.	35	10	15	35	50	mA
I_L	$I_G = 1.2\ I_{GT}$	I - III	MAX.	50	10	25	50	70	mA
		II		60	15	30	60	80	
dV/dt (2)	V_D = 67 %V_{DRM} gate open Tj = 125°C		MIN.	500	20	40	500	1000	V/µs
(dI/dt)c (2)	(dV/dt)c = 0.1 V/µs Tj = 125°C		MIN.	-	3.5	6.5	-	-	A/ms
	(dV/dt)c = 10 V/µs Tj = 125°C			-	1	2.9	-	-	
	Without snubber Tj = 125°C			6.5	-	-	6.5	12	

■ STANDARD (4 Quadrants)

Symbol	Test Conditions	Quadrant		BTA/BTB12		Unit
				C	B	
I_{GT} (1)	V_D = 12 V R_L = 30 Ω	I - II - III	MAX.	25	50	mA
		IV		50	100	
V_{GT}		ALL	MAX.	1.3		V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ Tj = 125°C	ALL	MIN.	0.2		V
I_H (2)	I_T = 500 mA		MAX.	25	50	mA
I_L	$I_G = 1.2\ I_{GT}$	I - III - IV	MAX.	40	50	mA
		II		80	100	
dV/dt (2)	V_D = 67 %V_{DRM} gate open Tj = 125°C		MIN.	200	400	V/µs
(dV/dt)c (2)	(dI/dt)c = 5.3 A/ms Tj = 125°C		MIN.	5	10	V/µs

STATIC CHARACTERISTICS

Symbol	Test Conditions			Value	Unit
V_T (2)	I_{TM} = 17 A tp = 380 µs	Tj = 25°C	MAX.	1.55	V
V_{to} (2)	Threshold voltage	Tj = 125°C	MAX.	0.85	V
R_d (2)	Dynamic resistance	Tj = 125°C	MAX.	35	mΩ
I_{DRM}	$V_{DRM} = V_{RRM}$	Tj = 25°C	MAX.	5	µA
I_{RRM}		Tj = 125°C		1	mA

Note 1: minimum IGT is guaranted at 5% of IGT max.

Note 2: for both polarities of A2 referenced to A1

THERMAL RESISTANCES

Symbol	Parameter			Value	Unit
$R_{th(j-c)}$	Junction to case (AC)		D^2PAK/TO-220AB	1.4	°C/W
			TO-220AB Insulated	2.3	
$R_{th(j-a)}$	Junction to ambient	S = 1 cm^2	D^2PAK	45	°C/W
			TO-220AB TO-220AB Insulated	60	

S = Copper surface under tab

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

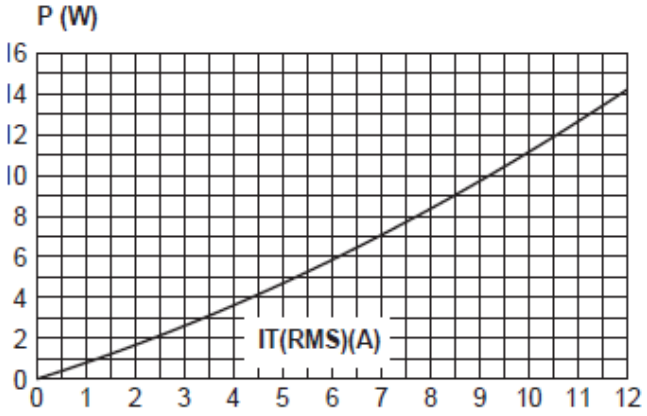


Fig. 2-1: RMS on-state current versus case temperature (full cycle).

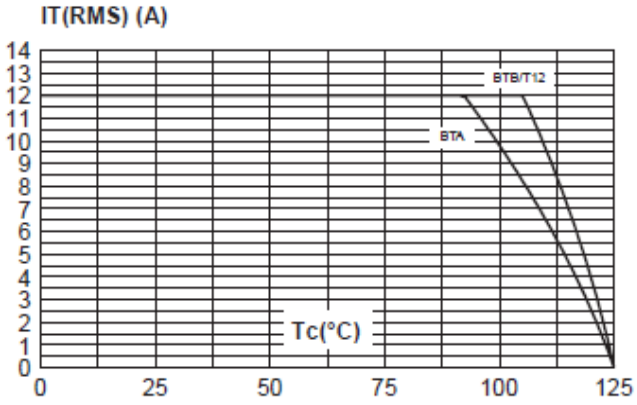


Fig. 2-2: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm),full cycle.

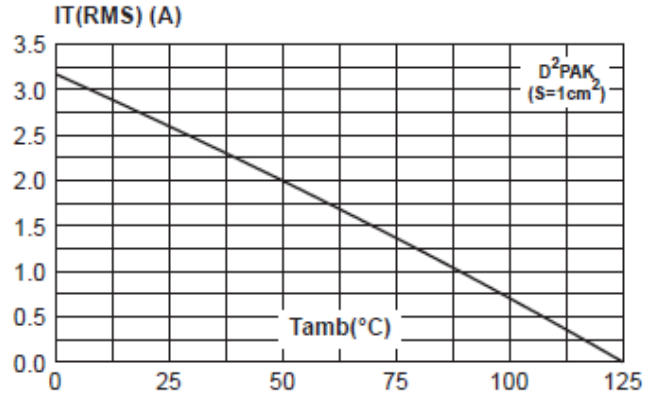


Fig. 3: Relative variation of thermal impedance versus pulse duration.

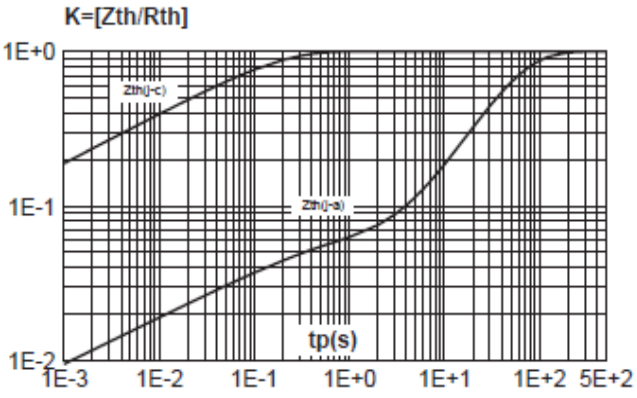


Fig. 4: On-state characteristics (maximum values).

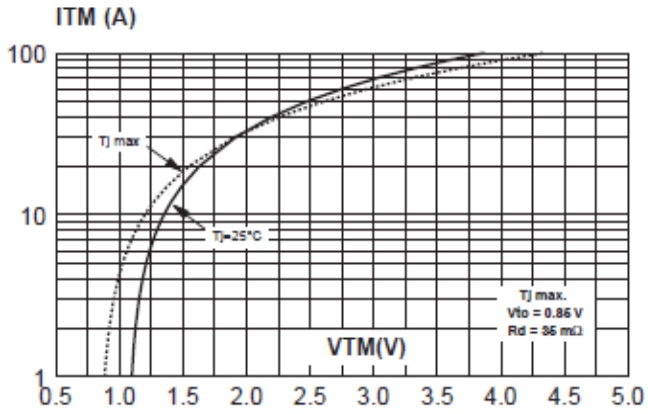


Fig. 5: Surge peak on-state current versus number of cycles.

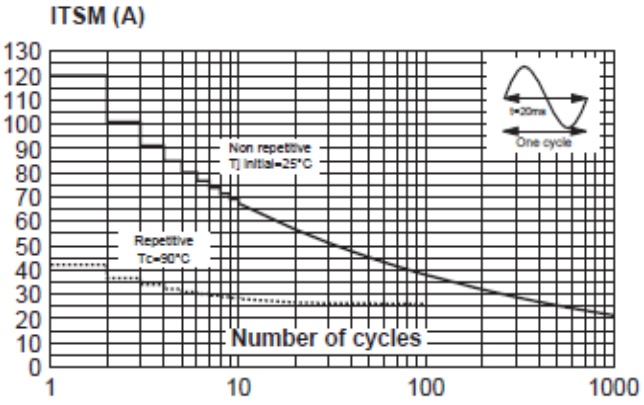


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10ms, and corresponding value of I^2t.

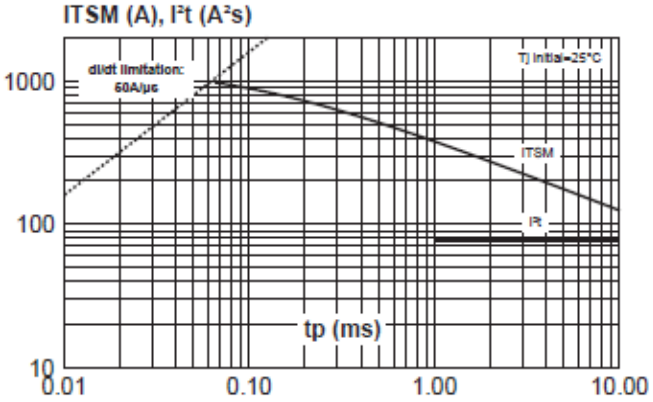


Fig. 7: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

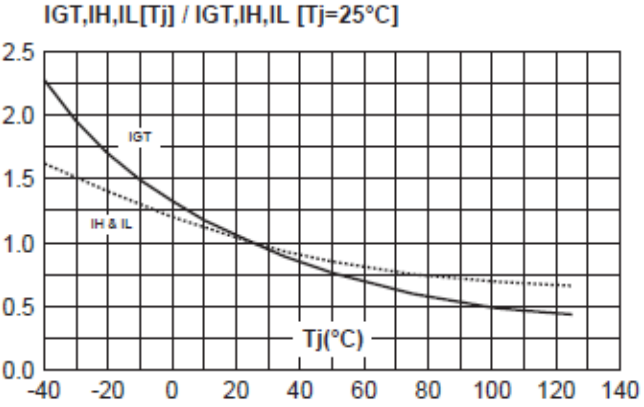


Fig. 8-1: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values) (BW/CW/T1235).

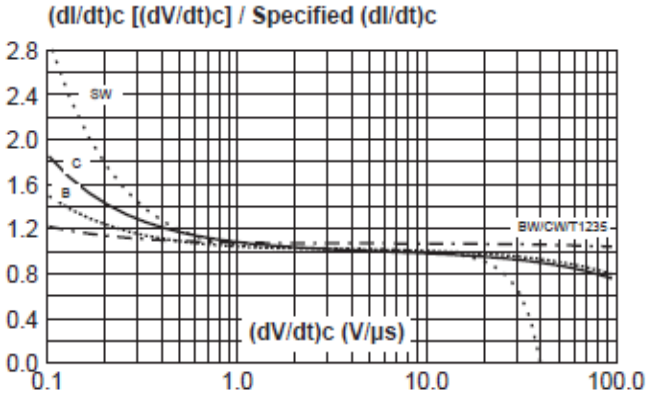


Fig. 8-2: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values) (TW).

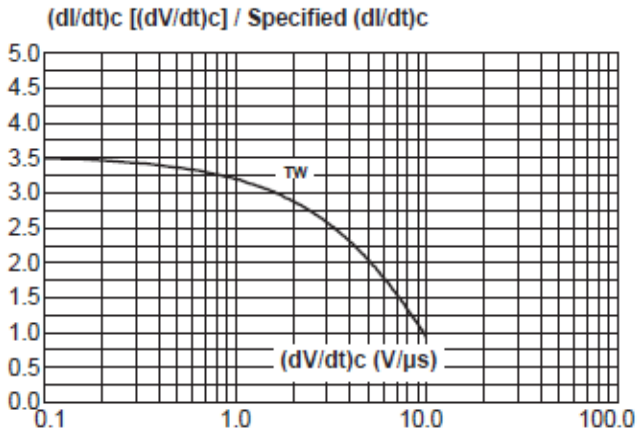


Fig. 9: Relative variation of critical rate of decrease of main current versus junction temperature.

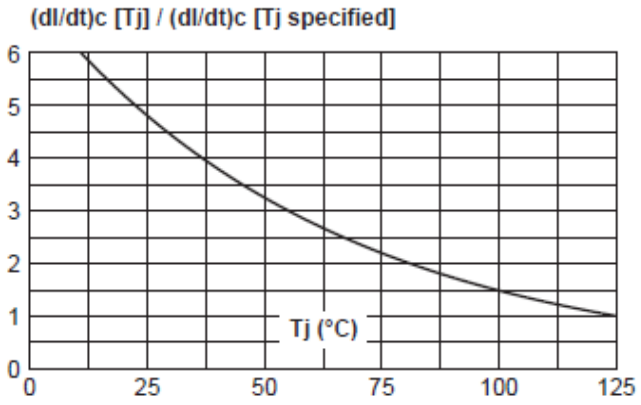


Fig. 10: D²PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 µm).