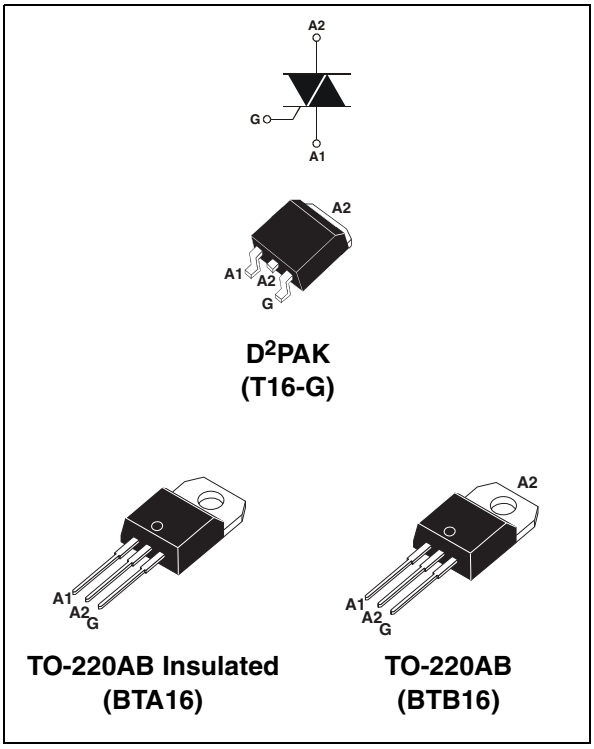
Table 1: Main Features

Symbol	Value	Unit
$I_{T(RMS)}$	16	A
V_{DRM}/V_{RRM}	600, 700 and 800	V
$I_{GT\ (Q_1)}$	10 to 50	mA



D²PAK (T16-G)

TO-220AB Insulated (BTA16)

TO-220AB (BTB16)

DESCRIPTION

Available either in through-hole or surface-mount packages, the **BTA16, BTB16** and **T16** triac series is suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control operation in light dimmers, motor speed controllers, ...

The snubberless versions (BTA/BTB...W and T16 series) are specially recommended for use on inductive loads, thanks to their high commutation performances. By using an internal ceramic pad, the BTA series provides voltage insulated tab (rated at 2500V_{RMS}) complying with UL standards (File ref.: E81734).

Table 2: Order Codes

Part Number	Marking
BTA16-xxxxxRG	See page table 8 on page 8
BTB16-xxxxxRG	
T16xx-xxxG	

Table 3: Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	D²PAK / TO-220AB	T_c = 100°C	16	A
		TO-220AB Ins.	T_c = 15°C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	F = 50 Hz	t = 20 ms	160	A
		F = 60 Hz	t = 16.7 ms	168	
I^2t	I^2t Value for fusing	t_p = 10 ms		144	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT} , $t_r \leq$ 100 ns	F = 120 Hz	T_j = 125°C	50	A/µs
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25°C	V_{DSM}/V_{RSM} + 100	V
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125°C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125°C	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	°C

Tables 4: Electrical Characteristics (T_j = 25°C, unless otherwise specified)

■ **SNUBBERLESS and Logic Level (3 quadrants)**

Symbol	Test Conditions	Quadrant		T16	BTA16 / BTB16			Unit
				T1635	SW	CW	BW	
I_{GT} (1)	V_D = 12 V R_L = 33 Ω	I - II - III	MAX.	35	10	35	50	mA
V_{GT}		I - II - III	MAX.	1.3				V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ T_j = 125°C	I - II - III	MIN.	0.2				V
I_H (2)	I_T = 500 mA		MAX.	35	15	35	50	mA
I_L	I_G = 1.2 I_{GT}	I - III	MAX.	50	25	50	70	mA
		II		60	30	60	80	
dV/dt (2)	V_D = 67 %V_{DRM} gate open	T_j = 125°C	MIN.	500	40	500	1000	V/µs
(dI/dt)c (2)	(dV/dt)c = 0.1 V/µs	T_j = 125°C	MIN.	-	8.5	-	-	A/ms
	(dV/dt)c = 10 V/µs	T_j = 125°C		-	3.0	-	-	
	Without snubber	T_j = 125°C		8.5	-	8.5	14	

■ **Standard (4 quadrants)**

Symbol	Test Conditions	Quadrant		BTA16 / BTB16		Unit
				C	B	
I_{GT} (1)	V_D = 12 V R_L = 33 Ω	I - II - III IV	MAX.	25 50	50 100	mA
V_{GT}		ALL	MAX.	1.3		V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ T_j = 125°C	ALL	MIN.	0.2		V
I_H (2)	I_T = 500 mA		MAX.	25	50	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	MAX.	40	60	mA
		II		80	120	
dV/dt (2)	V_D = 67 %V_{DRM} gate open	T_j = 125°C	MIN.	200	400	V/µs
(dV/dt)c (2)	(dI/dt)c = 7 A/ms	T_j = 125°C	MIN.	5	10	V/µs

Table 5: Static Characteristics

Symbol	Test Conditions			Value	Unit
V_T (2)	I_{TM} = 22.5 A t_p = 380 µs	T_j = 25°C	MAX.	1.55	V
V_{to} (2)	Threshold voltage	T_j = 125°C	MAX.	0.85	V
R_d (2)	Dynamic resistance	T_j = 125°C	MAX.	25	mΩ
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$	T_j = 25°C	MAX.	5	µA
		T_j = 125°C		2	mA

Note 1: minimum I_{GT} is guaranted at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1.

Table 6: Thermal resistance

Symbol	Parameter			Value	Unit
$R_{th(j-c)}$	Junction to case (AC)		D^2PAK / TO-220AB	1.2	°C/W
			TO-220AB Insulated	2.1	
$R_{th(j-a)}$	Junction to ambient	S = 1 cm^2	D^2PAK	45	°C/W
			TO-220AB / TO-220AB Insulated	60	

S = Copper surface under tab.

Figure 1: Maximum power dissipation versus RMS on-state current (full cycle)

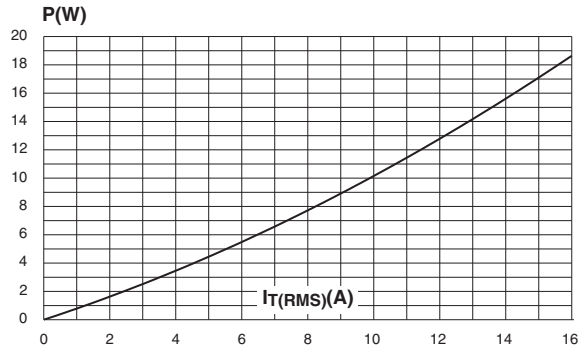


Figure 2: RMS on-state current versus case temperature (full cycle)

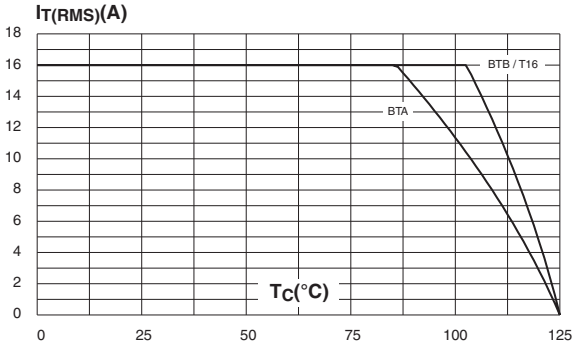


Figure 3: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm) (full cycle)

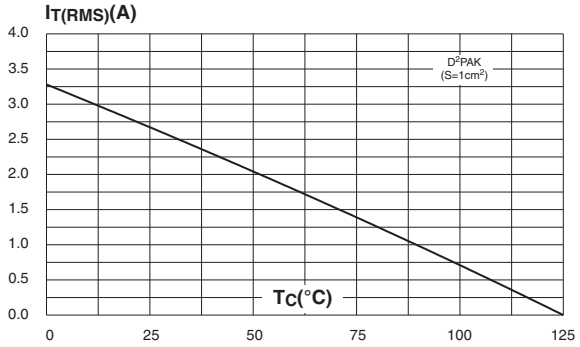


Figure 4: Relative variation of thermal impedance versus pulse duration

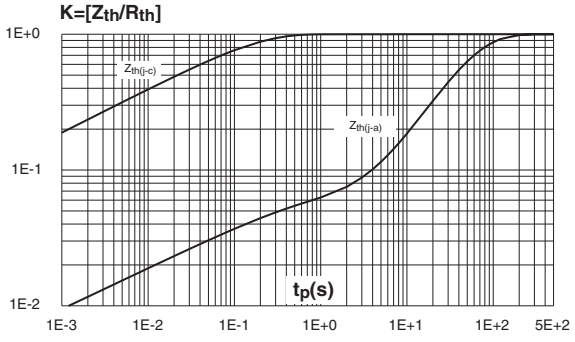


Figure 5: On-state characteristics (maximum values)

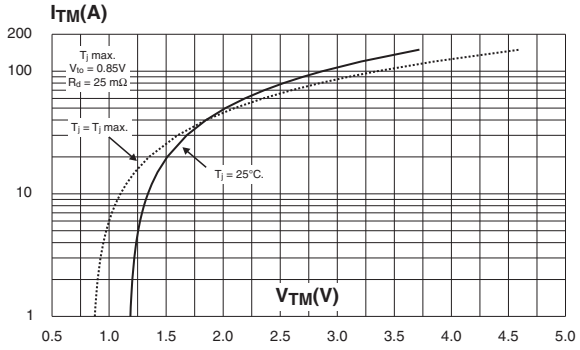


Figure 6: Surge peak on-state current versus number of cycles

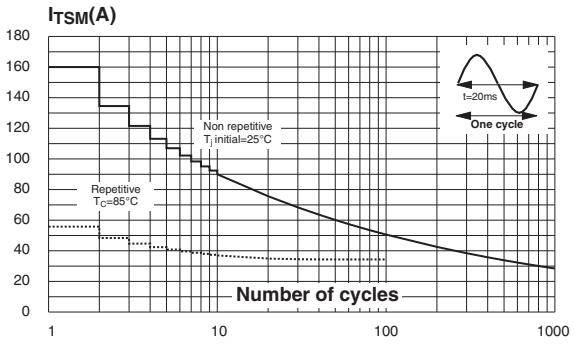


Figure 7: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms and corresponding value of I^2t

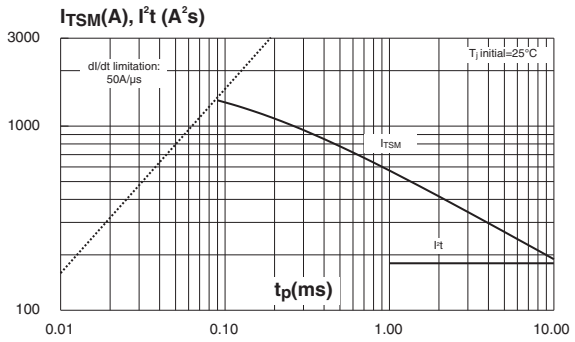


Figure 8: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

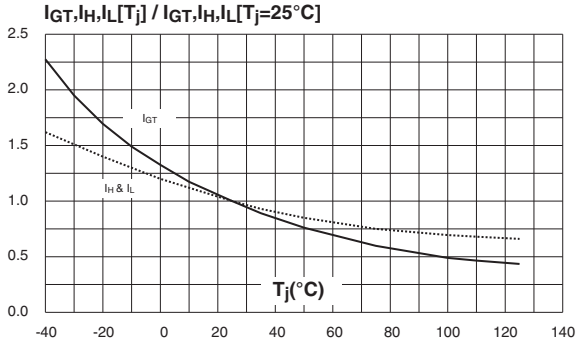


Figure 9: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values) (Snubberless & Logic level types)

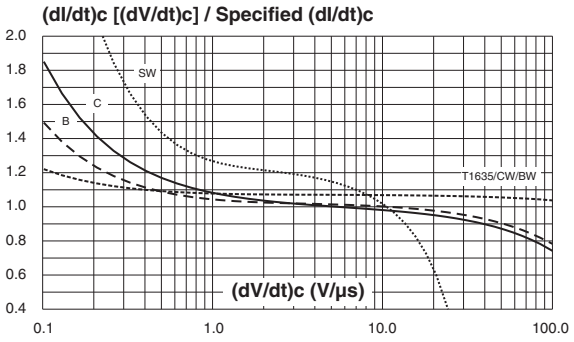


Figure 10: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values) (Standard types)

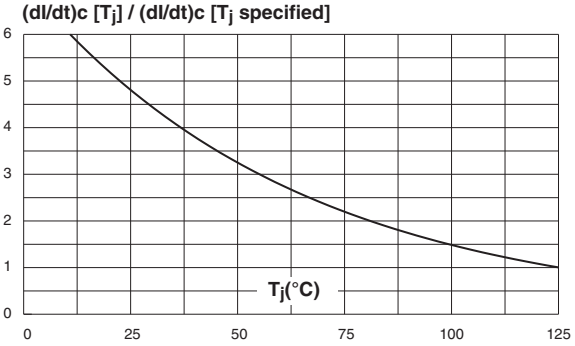


Figure 11: D^2PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 µm)